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Notice of References Cited	Application/Cont. No. 09/977,994	Applicant(s)/Patent Under Reexamination NAGATA ET AL	
	Examiner Jeffrey R. West	Art Unit 2857	Page 1 of 1

U.S. PATENT DOCUMENTS

★		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,144,217	11-2000	Iwata et al.	326/27
	B	US-4,366,456	12-1982	Ueno et al.	333/173
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

★		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

★		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nagata et al., "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits", Presented 05/21/00-05/24/00, Published IEEE Journal of Solid-State Circuits, 03/2001. Vol. 36, Issue 3, pp. 539-549.
★	V	Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment". Proceedings of the IEEE 1999 Custom Integrated Circuits Conference. May 1999.
★	W	Mitra et al., "Substrate-Aware Mixed-Signal Macrocell Placement in WRIGHT". IEEE Journal of Solid-State Circuits. Vol. 30. No. 3, March 1995.
★	X	Shimazaki et al., "LEMMINGS: LSI's EMI-Noise Analysis With Gate Level Simulator". Proceedings of the IEEE 2000 First International Symposium on Quality Electronic Design. March 2000.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.